LISTING OF CLAIMS:

Kindly cancel claims 1 to 16, without prejudice.

Kindly add claims as follows:

17. (New) A clock signal distribution device formed on a semiconductor substrate, comprising:

a clock input;

a first driver coupled to said clock input;

a second driver coupled to said clock input;

a first receiver coupled to said first driver by a first plurality of transmission lines;

a second receiver coupled to said second driver by a second plurality of transmission lines;

said first and second plurality of transmission lines being configured to provide substantially equal time delays;

said first receiver configured to provide a first output connected to a first site on a microprocessor; and

said second receiver configured to provide a second output connected to a second site on said microprocessor.

18. (New) A clock signal distribution device formed on a semiconductor substrate, as in Claim 17, wherein said semiconductor substrate comprises:

silicon germanium.

19. (New) A clock signal distribution device formed on a semiconductor substrate, as in claim 17, wherein said first and second plurality of transmission lines are configured to transmit both in phase and out of phase signals.

20. (New) A clock signal distribution device formed on a semiconductor substrate, as in claim 17, wherein said clock input is configured as a solder bump.

21. (New) A clock signal distribution device formed on a semiconductor substrate, as in claim 17, wherein said first and second outputs are configured as solder bumps.

22. (New) An integrated circuit device formed on a semiconductor substrate and configured to provide synchronized clock signals to multiple sites on a utilization device located external to the semiconductor substrate, comprising:

a clock input configured as a solder bump;

a first driver coupled to said clock input;

a second driver coupled to said clock input;

a first receiver coupled to said first driver by a first plurality of transmission lines;

a second receiver coupled to said second driver by a second plurality of transmission lines;

said first and second plurality of transmission lines being configured to provide substantially equal time delays;

said first receiver configured to provide a first output connected to a first site on a utilization device; and

said second receiver configured to provide a second output connected to a second site on said utilization device.

wherein said first and second outputs are configured as solder bumps connected to first and second sites on said utilization device.

23. (New) An integrated circuit device as in claim 22, wherein said integrated circuit device is formed on a silicon germanium substrate.

24. (New) An integrated circuit device as in claim 22, wherein said utilization device is a microprocessor.